4. CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 RF SWITCHING CIRCUIT (CTRL, RF AND PA UNITS)

The RF switching circuit leads receive signals to bandpass filters from an antenna connector while receiving. However, the circuit leads the signal from the RF power amplifier to the antenna connector while transmitting.

RF signals (on HF/6 m bands) from [ANT 1] or [ANT 2] pass through the antenna selector (CTRL unit; RL3), tuner switching relays (CTRL unit; RL1, RL2), transmit/receive switching relay (CTRL unit; RL4), and low-pass filter (CTRL unit; L27, L28, L35, C63–C67, C105, C115–C117), and are then applied to the RF unit via J2 (P2).

The signals from the CTRL unit bypass or pass through the 20 dB attenuator (RF unit; RL1, R1, R2). By selecting the attenuator, 0 (bypass) and 20 dB attenuations are obtained. The signals are then applied to the RF filters.

While operating on the 144 MHz band, the RF signals from the [144 MHz ANT] are passed through the low-pass filter (PA unit; L601–L603, C602, C604–C609) and transmit/receive switching relay (PA unit; RL601), then applied to the RF unit via J601 (P601).

4-1-2 RF FILTER CIRCUIT (RF UNIT)

The RF filter circuit contains 8 bandpass and 2 low-pass filters. Bandpass filters pass only the desired band signals and suppress any undesired band signals.

(1) 0.03–1.6 MHz

The signals are applied to the attenuator and low-pass filter directly (see above at right).

(2) 1.6–60 MHz

The signals pass through the high-pass filter (L2–L4, C4–C7) to suppress excessively strong signals below 1.6 MHz. The filtered signals are applied to a low-pass or one of 8 bandpass filters (see above at right).

(3) 108–174 MHz

The 144 MHz band signals are bypassed or passed through the attenuator (R122), then applied to the tunable bandpass filter (see above at right).

The filtered signals are applied to the pre-amplifier circuit.

• Used RF filter

Frequency range	Control signal	Input diode	Filter component
0.03–1.6 MHz	B0	D3	L11, L12, R11–R13, C12–C14, C17
1.6–2 MHz	B1	D21	L21–L23, C21–C25
2–4 MHz	B2	D31	L31–L33, C31–C35
4–8 MHz	B3	D41	L41–L43, C41–C45
8–11 MHz	B4	D51	L51–L53, C51–C55
11–15 MHz	B5	D61	L61–L63, C61–C65
15–22 MHz	B6	D71	L71–L73, C71–C75
22–30 MHz	B7	D81	L81–L84, C81–C85
30–50 MHz	B8W	D101	L101–L103, C101–C105
50–54 MHz	B8	D91	L91–L96, C90–C100
54–60 MHz	B8W	D101	L101–L103, C101–C105
108–174 MHz	B9R	None (via C500)	D501, L501, L502

4-1-3 PRE-AMPLIFIER CIRCUITS (RF UNIT)

A total of 3 pre-amplifier circuits are employed in the IC-746PRO/7400. 2 for HF/6 m bands and 1 for 144 MHz band operation.

When the pre-amplifier operation is turned OFF, the RF signals bypass this circuit.

When [P.AMP1] is selected, the filtered signals are applied to the pre-amplifier 1 circuit (Q181, Q182), which has 10 dB gain for the 1.8–54 MHz range, and when [P.AMP2] is selected, the signals are applied to the pre-amplifier 2 circuit (IC191), which has 16 dB gain for the 21–60 MHz range. The pre-amplified signals are applied to the 60 MHz cut-out low-pass filter (L210–L212, C211–215, C234).

During 144 MHz band operation, the filtered signals are pre-amplified at the VHF pre-amplifier (Q502) when the [P.AMP] is turned ON, and passed through the tunable bandpass filter (D502–D504, L503–L504).

The filtered signals are applied to the 1st mixer circuit.

4-1-4 1ST MIXER AND 1ST IF CIRCUITS (RF UNIT)

The 1st mixer circuit mixes the received signals with the 1st LO signal to convert the received signals into a fixed 64.455 MHz 1st IF signal.

The signals from the pre-amplifier circuit, or signals which bypass the pre-amplifier circuit, are applied to the 1st mixer (Q211, Q212) and mixed with the 1st LO signal (64.485–238.455 MHz) coming from the 1st LO PLL circuit via the LO amplifier (Q301) and low-pass filter.

The mixed 1st IF signal is passed through the MCFs (Monolithic Crystal Filter: FI231a/b) to suppress out-of-band signals. The filtered signal is amplified at the IF amplifier (Q241), and then applied to the 2nd mixer circuit.

When the bandscope function is activated, the 1st LO sweeping signal is supplied to the 1st mixer circuit.

4-1-5 2ND MIXER CIRCUIT (RF UNIT)

The 2nd mixer circuit converts the 1st IF signal into the 2nd IF frequency by mixing with the 2nd LO signal (64.00 MHz).

The 1st IF signal from the IF amplifier (Q241) is applied and converted into a 455 kHz 2nd IF signal at the 2nd mixer circuit (D261) by mixing with a fixed 64 MHz 2nd LO signal.

The 2nd IF signal is passed through the low-pass filter (L263, C262–C264) to suppress undesired signals such as the 2nd LO signal, and the applied to the MAIN unit via J261.

The 2nd LO signal is a doubled reference frequency, generated at the reference oscillator (X1901: 32.0 MHz) and doubled at Q1903 and Q1904.

4-1-6 NOISE BLANKER CIRCUIT (MAIN UNIT)

The noise blanker circuit detects pulse-type noise, and turns OFF the signal line when the noise appears.

The 2nd IF signal from the RF unit is applied to the noise blanker gate (D252, D253). A portion of the 2nd IF signal from RF unit is amplified at the noise amplifiers (Q200–Q203), and is then detected at the noise detector (D200) to convert the noise components to DC voltages.

The signal is then applied to the noise blanker switch (Q206, Q207). At the moment detected voltage exceeds Q206's threshold level, Q207 outputs a blanking signal to close the noise blanker gate (D252, D253). The PLL unlock signal are also applied to Q207 to control the noise blanker gate.

Some DC voltage from the noise detector circuit is fed back to the noise amplifiers (Q200, Q201) via the DC amplifiers (Q204, Q205). The DC amplifiers function as an AGC circuit to reduce average noise. Therefore, the noise blanker function shuts off pulse-type noise only.

4-1-7 2ND IF CIRCUIT (MAIN UNIT)

The 2nd IF circuit amplifies and filters the 2nd IF signal, and applies the 2nd IF signal to the 3rd mixer circuit.

The 2nd IF signal from the noise blanker gate (D252, D253) is amplified at the 2nd IF amplifier (Q250) and passed through the ceramic filters (FI271, FI272). The filtered signal is applied to the 3rd mixer circuit.

4-1-8 3RD MIXER AND 3RD IF CIRCUITS (MAIN UNIT)

The 3rd mixer circuit mixes the 2nd IF signal with the 3rd LO signal to obtain the 3rd IF (36 kHz) signal.

The 2nd IF signal from the ceramic filters (FI271, FI272) is applied to the 3rd mixer circuit (IC280, pin 1). The 3rd LO signal from the 3rd LO PLL circuit is also applied to the 3rd mixer (IC280, pin 5). The mixed signal is output from pin 6.

The 3rd IF signal is passed through the low-pass filter (IC1460a) and amplified at the 3rd IF amplifier (IC1460b). The filtered and amplified signal is then applied to the DSP unit via DRIF line.

4-1-9 DSP RECEIVER CIRCUIT (DSP UNIT)

The DSP (Digital Signal Processor) circuit enables digital IF filter, digital noise reduction, PSN (Phase Shift Network)/ Low Power/Phase demodulation, digital automatic notch, and etc.

The 36 kHz 3rd IF signal from the 3rd IF amplifier (MAIN unit; IC1460b) is amplified at the differential amplifiers (IC651a/b), and is then applied to the A/D converter section in the CODEC IC (IC501). At the same time, the converted signal is level-shifted 5V to 3.3 V in the IC (IC501).

The level-shifted signal is applied to the DSP IC (IC301) for the digital IF filter, demodulator, automatic notch and noise reduction, etc.

The output signal from the DSP IC is applied to the D/A converter section in the CODEC IC (IC501) to convert into the analog audio signals. Also the signals are level-shifted 3.3 V to 5V at the level converter section in the IC (IC501).

The level-shifted audio signals are passed through the active filter (IC701a), and then applied to the MAIN unit via J901 (pin 17) as the DRAF signal.

4-1-10 TWIN PBT CIRCUIT (DSP UNIT)

General PBT (Passband Tuning) circuit shifts the center frequency of IF signal to electronically narrow the passband width. The IC-746PRO/7400 uses the DSP circuit for the digital PBT function and actually shifts the both lower and higher passbands of 3rd IF filter within ±1.8 kHz.

The twin PBT circuit in DSP IC (IC301) controlled by the [TWIN PBT] controller adjusts the 3rd IF passband width and rejects interference.

4-1-11 AGC CIRCUIT (DSP UNIT)

The AGC (Automatic Gain Control) circuit reduces IF amplifier gain and attenuates IF signal to keep the audio output at a constant level.

The receiver gain is determined by the voltage on the AGC line (MAIN unit; IC1401, pin 14). The D/A converter for AGC (IC102) supplies control voltage to the AGC line and sets the receiver gain with the [RF/SQL] control.

The 3rd IF signal from the CODEC IC (IC501) is detected at the AGC detector section in the DSP IC (IC301). The output signal from the DSP IC (IC301) is level-shifted at the level converter (IC101) and applied to the D/A converter (IC102). The AGC voltage is amplified at the buffer amplifier section in IC102 and is applied to the MAIN unit to control the AGC line.

When receiving strong signals, the detected voltage increases and the AGC voltage decreases via the buffer amplifier (IC102). As the AGC voltage is used for the bias voltage of the IF amplifiers (RF unit; Q241, MAIN unit; Q250), IF amplifier gain is decreased.

4-1-12 SQUELCH CIRCUIT (MAIN UNIT)

The squelch circuit mutes audio output when the S-meter signal is lower than the [RF/SQL] setting level.

The NSQL or VSQL signal from the DSP unit is applied to the main CPU (IC1500) and is compared with the threshold level set by the [RF/SQL] control. The [RF/SQL] setting signal is passed through the sub CPU (DISPLAY board; IC1001, pin 91), and then applied to the main CPU. The main CPU analyzes the compared signal and outputs control signal to the squelch gate (IC1160, pin 5) to open or close the squelch as the SQLS signal.

4-1-13 AF AMPLIFIER CIRCUIT (MAIN UNIT)

The AF amplifier amplifies the audio signals to a suitable driving level for the speaker.

The AF signals (DRAF) from the DSP unit are passed through the squelch gate (IC1160) and amplified at the AF amplifier section of IC1180 (pins 2, 4), and volume is controlled by the AFGV signal at the VCA section (pins 7–9). The volume controlled AF signals are passed through the AF mute gate (IC1220, pins 7, 1), then applied to the AF power amplifier (IC1240, pin 1) via the ripple filter (Q1280).

The amplified audio signals are passed through the [PHONES] and [EXT SP] jacks then applied to the internal speaker when no plug is connected to the jacks.

The AF mute gate is controlled by the [AF] control via the sub and main CPUs.

4-1-14 TONE SQUELCH CIRCUIT (MAIN UNIT)

A portion of the detected FM audio signals from the DSP unit via the MONI line are amplified at the AF amplifier (IC1060). The amplified signals are applied to the low-pass filter (IC1001) to cut-out the 300 Hz or higher audio components, and subaudible tone signals only pass through. The filtered signal (subaudible tone) is then applied to the main CPU (IC1500, pin 108).

The main CPU detects the frequency of the applied subaudible tone signal and releases the audio mute when a matched tone frequency signal is detected.

4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT (MAIN UNIT)

The microphone amplifier circuit amplifies microphone audio signals to a level needed for the DSP circuit.

Audio signals from the [MIC] connector (MIC board; J1, pin 1) are amplified at the audio amplifier section in IC1400 (pins 2, 4), and then applied to the VCA section (IC1400, pin 7). The gain controlled signals are output from (IC1400, pin 9) and amplified at the AF amplifier (IC1401, pins 1–3) and passed through the low-pass filters (IC1401, pins 5–9) and analog switch (IC1310, pins 12, 14). The signals are then applied to the DSP circuit as the DTAF signal.

The VCA section in IC1400 (pins 7–9) controls microphone input gain according to the [MIC GAIN] control level using the MIGV signal coming from the main CPU via the I/O expander (IC502, pin 3).

4-2-2 VOX CIRCUIT (MAIN UNIT)

The VOX (Voice-Operated-Transmission) circuit sets transmitting conditions according to voice input.

When the VOX function is activated, a portion of the microphone signals are amplified at the VOX amplifier (IC1280 pins 3, 1) and applied to main CPU (IC1500, pin 109) via the VOXL line. A portion of the power amplified AF signals from the AF power amplifier (IC1240) are amplified at the anti-VOX amplifier (IC1121, pins 6, 7) and applied to the main CPU (IC1500, pin 110) via the AVXL line. Then the main CPU compares these and controls the transmitter circuit.

4-2-3 DSP TRANSMITTER CIRCUIT (DSP UNIT)

The DSP (Digital Signal Processor) circuit enables PSN (Phase Shift Network)/Low Power/Phase modulation, transmitter monitor, side tone, and etc.

The microphone audio signals from the MAIN unit via the DTAF line are amplified at the differential amplifiers (IC601a/b), and are then applied to the A/D converter section in the CODEC IC (IC501). At the same time, the converted signals are level-shifted 5 V to 3.3 V in the IC (IC501).

The level-shifted signal are applied to the DSP IC (IC301) and modulated at the DSP IC to produce the 36 kHz transmitter IF signal.

The modulated IF signal from the DSP IC is applied to the D/A converter section in the CODEC IC (IC501) to convert into the analog IF signal. Also the signal is level-shifted 3.3 V to 5V at the level converter section in the IC (IC501).

The level-shifted IF signal is passed through the active filter (IC701b), and then applied to the MAIN unit via J901 (pin 22) as the DTIF signal.

4-2-4 SPEECH COMPRESSOR CIRCUIT (DSP UNIT)

The speech compressor compresses the transmitter audio input signals to increase the average output level (average talk power).

When the speech compressor function is ON, the level-shifted signal from the CODEC IC (IC501) is applied to the DSP IC (IC301) and compressed at the DSP IC to obtain an average audio level.

At the same time, the compressed signals are modulated at the DSP IC and applied to the D/A converter section in the CODEC IC (IC501).

4-2-5 IF AMPLIFIER AND MIXER CIRCUITS (MAIN AND RF UNITS)

The modulated 3rd IF signal from the DSP unit (DTIF: 36 kHz) is amplified at the 3rd IF amplifier (MAIN unit; IC1120a) and passed through the low-pass filters (MAIN unit; IC1120b/c). The filtered signal is applied to the 3rd mixer circuit (MAIN unit; IC400, pin 1). The applied 3rd IF signal is mixed with the 3rd LO signal from the DDS circuit (RF unit; IC1601) to produce a 455 kHz 2nd IF signal.

The 2nd IF signal is output from pin 6 and passed through the ceramic bandpass filter (MAIN unit; FI381) for unwanted signals are suppressed. The filtered 2nd IF signal is amplified at the 2nd IF amplifier (MAIN unit; Q330). The amplified signal is applied to the 2nd mixer circuit on the RF unit via J250.

The 2nd IF signal is mixed with the 64 MHz 2nd LO signal, coming from the PLL circuit, at the 2nd mixer circuit (RF unit; D261) to obtain a 64.455 MHz 1st IF signal. The 1st IF signal is passed through the MCFs (RF unit; FI231b/a) to cutoff the undesired signals, and is then amplified at the 1st IF amplifier (RF unit; Q271) via the T/R switch (RF unit; D251). The amplified 1st IF signal is applied to the 1st IF mixer circuit (RF unit; D271) via the attenuator (RF unit; D272) and low-pass filter circuit.

The operating (transmitting) frequency is produced at the 1st IF mixer circuit (RF unit; D271) by mixing the 1st IF and 1st LO signals. The mixed signal is then applied to the RF circuit.

4-2-6 RF CIRCUIT (RF AND PA UNITS)

The RF circuit amplifies operating (transmitting) frequency to obtain 100 W of RF output.

The signal from the 1st IF mixer is passed through one of the low-pass or bndpass filters (Refer to page 4-1 for bandpass filters used) and high-pass filters after passing through the low-pass filter (RF unit; L285, L286, C286–C289, C291). The filtered RF signal is amplified at the wide-band YGR amplifier (RF unit; IC151), and is then applied to the PA unit via J151.

The signal applied from the RF unit is amplified at the 2 predrive (PA unit; Q1, Q2) and drive (DRV board; Q1, Q2) amplifiers. These amplifiers cover all HF, 50 MHz and 144 MHz band amplifying operation.

When operating on the HF or 50 MHz band, the signal from the drive amplifier is power amplified at the HF/50 MHz power amplifier (PA unit; Q5, Q6) via the band switching relay (PA unit; RL2). However, the 144 MHz signal is power amplified at the 144 MHz power amplifier (PA unit; Q201, Q202) to obtain a stable 100 W of RF output power.

The amplified signal is applied to the desired antenna connector via one of 8 low-pass filters.

4-2-7 ALC CIRCUIT (MAIN UNIT)

The ALC (Automatic Level Control) circuit controls the gain of IF amplifiers in order for the transceiver to output a constant RF power set by the [RF PWR] control even when the supplied voltage shifts, etc.

The RF power level is detected at the SWR detector circuit (HF/50 MHz bands: CTRL unit; D2, 144 MHz band: PA unit; D602) to be converted into DC voltage and applied to the MAIN unit as the FOR (HF/50 MHz) or VFOR (144 MHz) signal.

The FOR or VFOR signal is applied to the comparator (IC300, pin 6). The POCV signal, controlled by the [RF PWR] control via the I/O expander (IC502, pin 4), is also applied to the other input (pin 5) for reference. The compared signal is output from pin 7 and applied to the IF amplifiers in the MAIN (Q330) and RF (Q271) units to control amplifying gain.

When the FOR or VFOR signal exceeds the POCV voltage, ALC bias voltage from the comparator controls the IF amplifiers. This adjusts the output power to a specified level from the [RF PWR] control until the FOR (VFOR) and POCV voltages are equalized.

In AM mode, the comparator operates as an averaging ALC amplifier. Q304 turns ON and the POCV voltage is shifted for 40 W AM output power (maximum) through R320.

The ALC bias voltage is also applied to the ALC meter amplifier (IC300, pin 2) to obtain an ALC meter signal (ALCL). The amplified signal is passed through the analog switch (IC 1900, pins 5, 4) and applied to the main CPU (IC1500, pin 107) to drive the S/RF meter via the sub CPU (IC1001) on the DISPLAY board.

An external ALC input from the [ALC] jack or [ACC] sockets is applied to the buffer amplifier (Q307). External ALC operation is identical to that of the internal ALC.

The FOR or VFOR signal is also applied to the power meter amplifier (IC360, pin 3). The amplified signal is applied to the main CPU (IC1500) after being switched by the analog switch (IC1900, pins 12, 14) as an FORL signal to drive the S/RF meter via the sub CPU (DISPALY board; IC1001).

4-2-8 APC CIRCUIT (MAIN UNIT)

The APC (Automatic Power Control) circuit protects the power amplifiers on the PA unit from high SWR and excessive current.

The reflected wave signal appears and increases when the connected antenna is mismatched to 50 Ω. The SWR detector circuit (HF/50 MHz bands; CTRL unit; D1, 144 MHz band; PA unit; D603) detects the reflected signal, and applies it to the APC circuit (IC300, pin 9) as a REF (HF/50 MHz) or VREF (144 MHz) signal.

When the REF or VREF signal level increases, the APC circuit decreases the ALC voltage to activate the APC.

For the current APC, the power transistor current is obtained by detecting the voltages (ICH and ICL) which appear at both terminals of the current detector (PA unit; R28). The detected voltages are applied to the differential amplifier (IC300, pins 12, 13). When the current of transistors is increased, the amplifier controls the ALC line to prevent excessive current flow.

A portion of the REF or VREF signal is applied to the SWR meter amplifier (IC360, pin 5). The amplified signal is applied to the main CPU (IC1500) after being switched by the analog switch (IC1900, pins 2, 15) as an REFL signal to drive the SWR meter.

4-3 PLL CIRCUITS

4-3-1 GENERAL

The PLL circuits generate a reference frequency (32.000 MHz); 1st LO frequencies (64.485–238.455 MHz); 2nd LO frequency (64 MHz), 3rd LO frequency (419.000 kHz).

The 1st LO PLL adopts a mixer-less dual loop PLL system and has 4 VCO circuits which cover from 30 kHz to 174 MHz. The 1st LO and 3rd LO use DDSs, while the 2nd LO uses the fixed frequency of the crystal oscillator.

4-3-2 1ST LO PLL CIRCUIT (RF UNIT)

The 1st LO PLL contains a main and reference loop as a dual loop system.

The reference loop generates an approximate 10.8 MHz frequency using a DDS circuit, and the main loop generates a 64.485 to 238.455 MHz frequency using the reference loop frequency.

(1) REFERENCE LOOP PLL

The oscillated signal at the reference VCO (Q1301, D1301) is amplified at the amplifiers (Q1302, Q1102) and is then applied to the DDS IC (IC1101, pin 46). The signal is then divided and detected on phase with the DDS generated frequency.

The detected signal output from the DDS IC (pin 56) is converted into DC voltage (lock voltage) at the loop filter (R1135, R1138, C1121) and then fed back to the reference VCO circuit (Q1301, D1301).

(2) MAIN LOOP PLL

The oscillated signal at one of the main loop VCOs (VCO board, Q1201, D1201, Q1221, D1221, Q1241, D1241, Q1261, D1261) is amplified at the buffer amplifiers (PLL board, IC1802, Q1281) and is then applied to the PLL IC (IC1801, pin 4). The signal is then divided and detected on phase with the reference loop output frequency.

The detected signal output from the PLL IC (pin 13) is converted into a DC voltage (lock voltage) at the loop filter and then fed back to one of the VCO circuits (VCO board, Q1201, D1201, Q1221, D1221, Q1241, D1241, Q1261, D1261).

The oscillated signal from the buffer amplifier (IC1802) is also applied to the MAIN unit as a 1st LO signal after being doubled or passed through the low-pass filter.

4-3-3 2ND LO AND REFERENCE OSCILLATOR CIRCUITS (RF UNIT)

The reference oscillator (X1901, Q1901) generates a 32.0 MHz frequency for the 2 DDS circuits as a system clock and for the LO output. The oscillated signal is doubled at the doubler circuit (Q1903, Q1904) and the 64.0 MHz frequency is picked up at the double tuned filter (L1903, L1904). The 64.0 MHz signal is applied to the RF circuit as a 2nd LO signal.

4-3-4 3RD LO CIRCUIT (RF UNIT)

The DDS IC (IC1601) generates a 10-bit digital signal using the 32 MHz system clock. The digital signal is converted into an analog wave signal at the D/A converter (R1601–R1620).

The converted analog wave is passed through the bandpass filter (L1602, L1603, L1605, C1609–C1613, C1615–C1617) and then applied to the MAIN unit as the 3rd LO signal (491.000 kHz).

4-3-5 MARKER CIRCUIT (RF UNIT)

The divided signal at the DDS circuit (IC1101) is used for the marker signals with the IC-746PRO/7400.

The reference signal for the DDS circuit (32.0 MHz) is divided by 2 to produce an acceptable frequency signal, 16 MHz, with the programmable divider then divided again by 160 to obtain 100 kHz cycle square-wave signals.

The generated marker signals are output from pin 49 of the DDS IC (IC1101) and then applied to the 1st mixer circuit (Q211, Q212) via the marker switch (IC1081) as the MKR signal.

4-4 ANTENNA TUNER CIRCUITS

4-4-1 MATCHING CIRCUIT (TUNER UNIT)

The matching circuit is a T-network. Using 2 tuning motors, the matching circuit obtains rapid overall tuning speed.

Using relays (RL1–RL15), the relay control signals from the antenna tuner CPU (CTRL unit; IC5) via the buffer amplifier (Q1–Q15) ground one of the taps of L3–L9, L11, L12 and add capacitors (C34–C43). After selecting the coils and capacitors, 2 motors (MF1, MF2) adjust C44 and C45 using the antenna tuner CPU (CTRL unit; IC5) and the motor driver circuit (CTRL unit; Q211–Q218) to obtain a low SWR (Standing Wave Ratio).

4-4-2 DETECTOR CIRCUITS (CTRL UNIT)

(1) SWR detector

Forward and reflected power are picked up by a current transformer (L1), detected by D1 and D2, and then amplified at IC1b and IC1a, respectively. The amplified voltages are applied to the antenna tuner CPU (IC5, pins 2, 3). The antenna tuner CPU detects the SWR.

(2) Reactance components detector

Reactance components are picked up by comparing the phases of the RF current and RF voltage. The RF current is detected by L4 and R16, and rectified at D5 and amplified at the C-MOS inverter amplifier (IC14e) and buffer amplifier (IC2a). The amplified signal is then applied to the phase comparator (IC3a). RF voltages are detected by C12–C14 and rectified at D4, and amplified at the C-MOS inverter amplifier (IC14c). The amplified signals are then applied to the phase comparator (IC3b) after being amplified at the buffer amplifer (IC2b). The output signal from the phase comparator (IC3a, pin 6 for RF current, IC3b pin 7 for RF voltage) is rectified at D7 and D6 for conversion into DC voltage. The rectified voltage signals are combined, then amplified at IC4b, then applied to the antenna tuner CPU (IC5, pin 64).

A C-MOS inverter IC is used for the buffer-amplifier (IC14) to improve functionable sensitivity. The C-MOS inverter amplifier is very responsive, and ensure quick and stable signal detection, even at a low RF signal level input.

(3) Resistance components detector
Resistance components are picked up by L8, and detected by D8, D9 and Q5. The detected resistance components are amplified at the amplifier (IC4a), and then applied to the antenna tuner CPU (IC5, pin 1).

4-4-3 MOTOR CONTROL CIRCUIT

The control circuit of the internal antenna tuner consists of the CPU, EEPROM*, tuning motors and tuning relays.
*Electronically-Erasable Programmable Read Only Memory

(1) CPU and EEPROM (CTRL unit)
The antenna tuner CPU (IC5) controls the tuning motors via the motor driver circuit (Q211–Q218) and tuning relays directly, and memorizes the best preset position in 100 kHz steps. The memory contents are stored in the EEPROM (IC6) without a backup battery.

(2) Tuning motors (CTRL unit)
The motor driver circuit (Q211–Q218) rotates the tuning motors (MF1, MF2) to obtain a low SWR.

(3) Tuning relays (TUNER unit)
According to the operating frequency band and antenna condition, tuning relays select the capacitors (C34–C43) and coils (L3–L9, L11, L12).